A DC to X-Band Frequency Doubler Using GaAs HBT MMIC

Xiangdong Zhang, and Yong-Hoon Yun

Corporate R &D Center, M/A-COM Inc.
100 Chelmsford St. Lowell, MA

Abstract— An analog frequency doubler is developed using GaAs HBT MMIC technology. In this doubler circuit, a novel push-push circuit configuration is used to provide the efficient frequency conversion and the fundamental frequency rejection over a broad bandwidth. The measurement results of the MMIC demonstrate an average 0 to 3 dB conversion gain and a 10 dB rejection on fundamental frequency up to 14 GHz. Thus, this MMIC can be used as a low-cost insertion block to achieve any stable local-oscillation signals up to X-band by multiplying the high quality VCOs at low frequencies, especially the inexpensive Si BJT based VCOs at wireless frequencies.

I. INTRODUCTION

AS THE FREQUENCY for wireless communications extends to higher and higher frequency bands, such as C-band and X-band for wireless LAN, to generate highly stable local oscillation (LO) signals with low cost becomes more and more challenging due to the frequency limitation of Si BJTs and surface-mount-circuits technology. The use of frequency doublers and multipliers can be a practical and quick solution to generate high quality LOs from the well developed VCOs at frequencies below 3GHz. This solution, however, requires the doubler/multiplier to be 1) broadband to cover all the possible application frequencies, 2)simple to use, and 3)low-cost, while maintaining good performance in frequency conversion efficiency and rejection on fundamental frequency.

The conventional diode/transistor based frequency doubler or multiplier is not a suitable solution for the above requirements due to their complicated circuit, the difficulty in circuit design, and relatively narrow bandwidth in most of the circuits[1- 3]. Therefore, an HBT MMIC doubler is developed to overcome the short-comings of the conventional approaches and to satisfy the requirements for low cost doublers/multipliers. This circuit combines the advantages of: 1) a novel push-push doubler circuit topology; 2) the high frequency performance of GaAs HBT; and 3) a low cost HBT MMIC process.

II. THE CIRCUIT TOPOLOGY

As shown in the schematic of the MMIC doubler in Fig.1, it can be divided into three portions: 1) a push-push common-collector pair to provide the frequency doubling function for sinusoidal signals; 2) the phase shifter which provides 180° phase shift over broad bandwidth using a differential amplifier with single-ended input; 3) the common-collector (emitter-follower) driving stage to provide power on low impedance loads. The circuit requires a single power supply at 5V. The RF ground path is provided by the two capacitors at the Vcc port and one of the input port in differential amplifier stage.

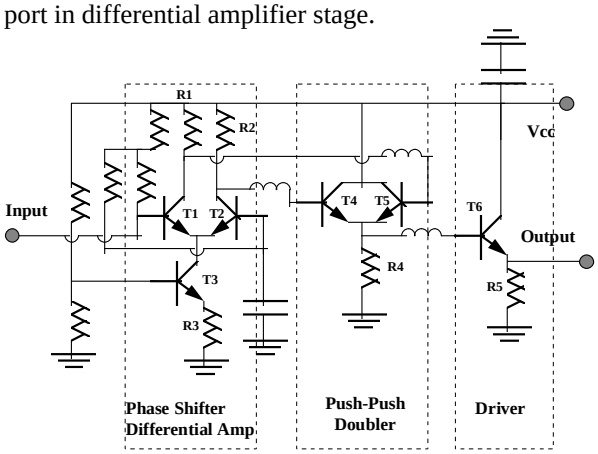

Fig.1. The circuit schematic of the MMIC doubler

The design goal of the circuit is to achieve 0 to 3dB conversion gain and 10 dB fundamental rejection up to 14 GHz. Choosing such low conversion gain is to ease the power leveling when the MMIC is used to construct a multiplication chain in a cascade fashion. The doubler circuit performance was simulated on Libra nonlinear simulator using the large-signal model

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of M/A-COM HBTs, which has been validated and reported by Wu. et al.[5].

The resistors value in the circuit is designed to provide not only the appropriate RF load but also the bias condition for all the six HBT transistors. In this way, the need for any DC block and RF choke between transistors is eliminated to achieve a broadband and simple circuit. The inductors are used to compensate capacitance effect of the transistors to obtain relatively flat frequency response over a wide frequency range.

III. THE OPERATING PRINCIPLE OF THE PUSH-PUSH CIRCUIT

The key portion in this MMIC is the push-push frequency doubler. Its operating principle is described conceptually in the diagram in Fig.2. The phase shifter in front of the push-push doubler provides signals to the transistors T4 and T5 with 180 degree phase difference. When the voltage at node "1" reaches to the positive half cycle, T4 is turned on and T5 is turned off. A current then flows through T4 toward the output load resistor, thus voltage at node "3" rises and falls following the voltage waveform at node "1". Wise versa, during the time period "t1" to" t2", T4 is turned off, and T5 is on, then the output waveform follows the positive voltage cycle at base of T5. Since the output waveform is exactly the same during the first and the second half cycle of the input signal, the output signal's frequency is twice of that in the input signal. As an analogy, this circuit can also be understood as an "active full-wave rectifier".

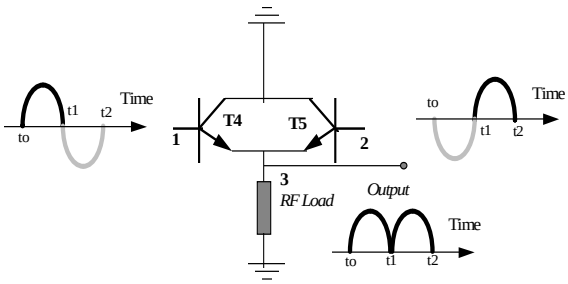


Fig. 2. The frequency doubler using an HBT emitter follower pair.

The use of common-collector configuration in the circuit minimizes the effect of the base-emitter junction capacitors at high frequency. Comparing to the traditional common emitter push-push approach [4], the new circuit has broad bandwidth and high frequency conversion efficiency.

IV. HBT DEVICE AND THE MMIC

The 2-finger HBT (2x3μmx10μm) is used to realize the doubler circuit design, of which the f_T is 40GHz. A self-aligned mesa-etching HBT process was developed to assure the low cost and the good performance. In the MMIC, there are two types of resistors used: 1) NiCr resistors used for relatively high resistance value with small current, such as the base bias resistors; 2) sub-collector(22Ω/) resistor is used for the low resistance with high current density (R1 to R5 in Fig.1).

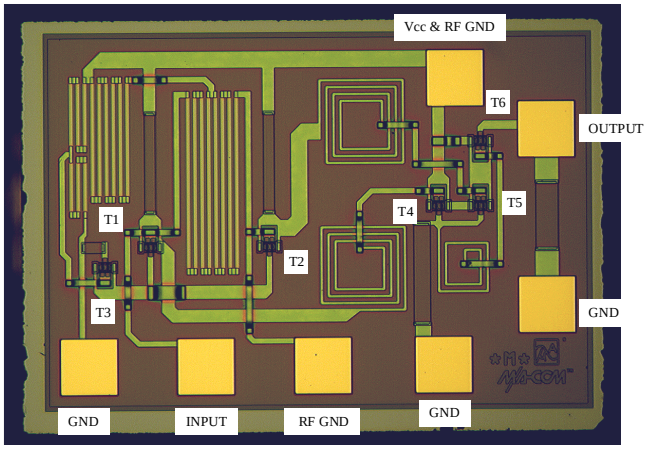


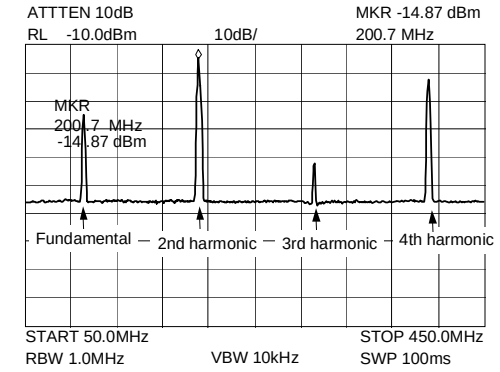
Fig. 3. The photo copy of the HBT MMIC doubler.

The dimension of the MMIC is 1.0X0.7mm^2. As seen in the photo copy of the HBT MMIC in Fig.3, the spiral inductors are for the frequency compen-sation, the mender-line resistors are for the base bias of three transistors in the differential amplifier. There are 7 bond-pads used in the MMIC for the purpose of I/O connection and the on-wafer probe. The two RF ground capacitors are designed to be outside of the chip to save the die-size. Notice that: since the ground path is provided by the off-chip capacitors, there is no need to use the via hole for low parasitic ground in this circuit. Therefore, the via-hole is avoided in this MMIC process to help reducing the cost further.

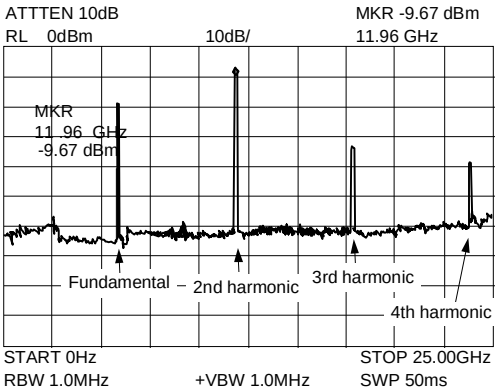
V. PERFORMANCE OF THE PROTOTYPE MMIC

The prototype MMIC chip was mounted in an R-380 package to test the performance. The chip-capacitors for DC block at input/output and RF short capacitors were also assembled together to the HBT MMIC die in the package via bond-wires. The bias for

the MMIC was 65mA at 5V. To measure the frequency response, a CW signal at power level of -3dBm was input at the MMIC at varying frequencies. The harmonics of output signal of the MMIC were monitored by a spectrum analyzer.



(a)



(b)

Fig. 4. The output power spectrum of the frequency doubler MMIC with (a) 200MHz and (b) 12GHz output frequencies, respectively. There is a 6dB attennuator after the doubler circuit.

As shown in Fig.4, the doubler demonstrates an efficient frequency conversion and high fundamental rejection at the output frequencies as low as 200MHz, and as high as 12 GHz. In Fig. 5. the output power level at harmonic frequencies up to 4th order is displayed as a function of the frequency of the input CW signal. Clearly the second harmonic output is the most significant harmonic over the input frequency range from 100MHz to 7 GHz. The output power roll-off at the frequencies lower than 1GHz is due to the frequency response of the DC block capacitors. The fundamental output, as well as the 3rd and 4th harmonics, are lower than the second harmonic by 10 dB except a few resonant points. The inceasing in output power at 4GHz input frequency is caused by the parasitic capacitance resonating with the frequency-compensation inductors, and the ripples in the other harmonics are due to the same resonant. This parasitic capacitance will be improved by a slight layout change in the next design iteration.

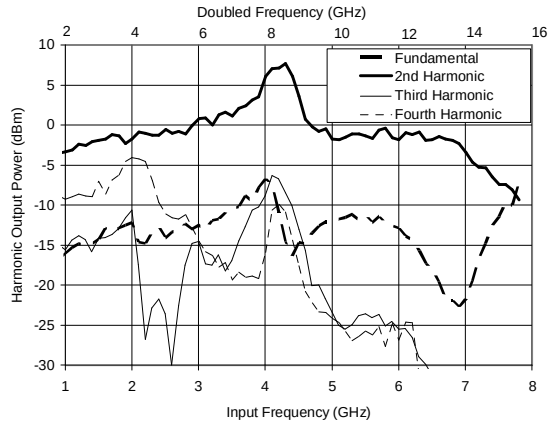


Fig. 5. The output power of the doubler MMIC ar all the harmonics with -3 dBm input power.

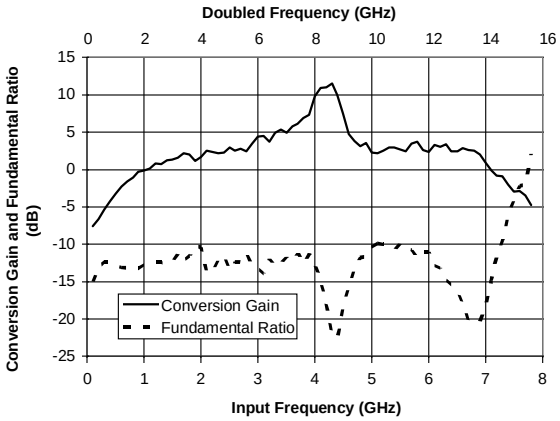


Fig. 6. The frequency conversion gain and the fundamental power ratio at output.

The calibrated frequency conversion gain and the rejection on fundamental frequency of the prototype MMIC are depicted in Fig.6. With the -3dBm input power, a frequency conversion gain is achieved in the MMIC for the output frequencies from 2 to 14 GHz. The average conversion gain of 2dB in 50Ω system is designed for the convenience in building cascade multiplication chain. The fundamental rejection in the figure is defined as the ratio between the output fundamental signal power and the second harmonic output power. (which is usually referred to as "subharmonic spurious signal level"). The rejection on the fundamental signal is better than 10 dB up to 14GHz, which is solely due to the novel push-push circuit configuration.

VI. DEMONSTRATION A QUADRUPLER USING THE DOUBLER MMICs

By cascading two doubler MMICs, a frequency quadrupler was realized in a R-380 package. As shown in Fig. 7, the two MMICs are simply put together in series and with a DC block capacitor in between. This frequency quadrupler circuit then was measured in the 50Ω system for the frequency conversion performance. Fig. 8. shows an example of the output power spectrum of the circuit with a 2.8GHz input at -11dBm to generate an 11.2GHz signal. A 10 dB attenuator was used at the output. Clearly, the 4th harmonic is the dominant frequency component at the output, and the rejection on the fundamental signal is better than 12 dB. However, the rejection on the 2nd and the 3rd harmonic is only a few dB due to the non-sinusoidal input at the second stage MMIC. This rejection can be improved using the appropriate LC network between the two MMIC instead of a simple large value capacitor. In Fig.9, the frequency conversion performance of the frequency quadrupler is depicted as a function of input signal frequency. The average conversion gain for the output from 4 to 13GHz is about 6dB. This demonstration clearly shows that by cascading two MMICs, one can achieve low cost stable LO source at any frequencies up to X band by quadrupling Si BJT VCOs at frequencies below 3 GHz.

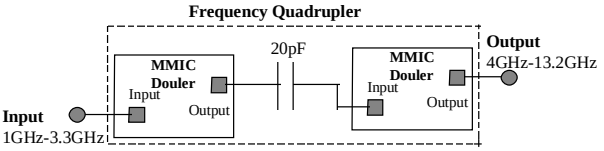


Fig. 7. The Conceptual block diagram of a frequency quadrupler using two frequency doubler MMICs.

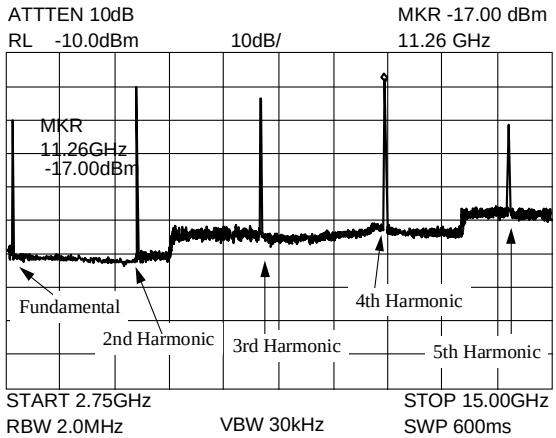


Fig. 8. The output power spectrum of a frequency quadrupler using HBT MMICs. A 10 dB attenuator was used at the output of the circuit.

Conclusions: An HBT based MMIC frequency doubler circuit has been successfully developed using a push-push circuit topology. This prototype MMIC is capable to provide efficient frequency conversion and high fundamental rejection from 200MHz to 14 GHz at the output. A frequency quadrupler was also demonstrated in this paper by cascading two MMICs. The MMIC can be packaged in the low cost package to be a surface-mount building block to help in achieving low-cost, high frequency stability at high end of wireless frequency.

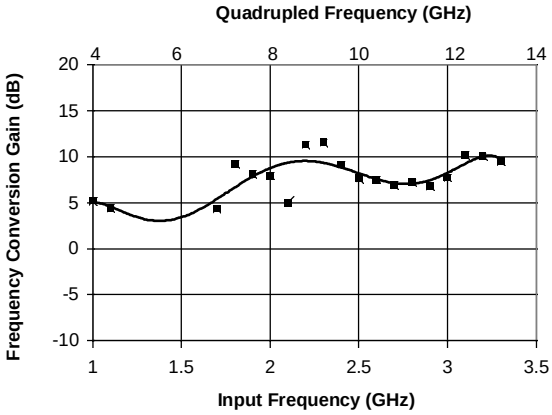


Fig. 9. The frequency conversion gain of the quadrupler as a function of frequency. The input power is -11dBm.

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